# 30th IEEE WORKSHOP ON SIGNAL AND POWER INTEGRITY

PROCEEDINGS

IEEE · IEEE Electronics Packaging Society · EMC Society · MTT-S IEEE Microwave Theory & Technology Society · Politecnico di Torino | DET

# 2026 IEEE 30th Workshop on Signal and Power Integrity (SPI)

## PROCEEDINGS

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Dear Friends and Colleagues,

We are delighted to present the Proceedings of the **30th IEEE Workshop on Signal and Power Integrity**!

For three decades now, SPI has stood as a premier global forum, bringing together minds from around the world to exchange groundbreaking ideas on all aspects of Signal and Power Integrity. As modern high-speed designs escalate in complexity, the specialized expertise fostered within our community is more critical than ever. To meet this challenge, we curated a comprehensive technical lineup for this landmark anniversary event, which took place from June 14th to 17th in Turin, Italy.

**SPI 2026** brought together 117 participants from 20 countries across Europe, the Americas, and Asia, featuring a rich and diversified technical program with 55 presentations in total:

– An insightful, highly anticipated Keynote presentation by Kaladhar Radhakrishnan (Intel Fellow) on *Breaking the AI Power Wall – An Overview of the Challenges and Solutions*.

– 7 outstanding presentations at the inaugural Global SIPI University course, skillfully led by Co-Chairs Christian Schuster and Francesco de Paulis, with a superb lineup of industry-leading instructors: Xiaomin Duan, Andreas Hardock, Wendem Beyene, Giordano Mariani, Gianni Signorini, and Aman Gupta.

– 33 oral presentations, divided across 8 high-quality core technical sessions, and 14 poster presentations in a dedicated interactive session, showcasing the latest research outcomes and industrial applications in the field.

To honor our history, a 30th Anniversary Special Session brought together members of the SPI Standing Committee to share exclusive insights and testimonials celebrating the workshop's enduring legacy and success. This milestone also provided a meaningful opportunity to pay a well-deserved tribute to one of the pioneers of this conference: Prof. Flavio Canavero, now retired, who has dedicated his leadership and expertise to SPI since its very first edition in 1997.

Following the workshop's established academic high standards, the **SPI 2026 Awards & Grants** recognized outstanding contributions to encourage continued research within our global community. We extend our congratulations to this year's recipients:

– **Best Paper Award**: Tim Pattyn, for the work titled *A Novel Vectorial Unified Transform for the Full-Wave Broadband Characterization of On-chip Passives*.

– **Best Student Paper Award**: Atacan Tuhan, for the work titled *A Scalable Distributed Electromagnetic Solver for 3D Integrated Circuit Design*.

– **Best Poster Award**: Nazanin Soleimani, for the work titled *Compressed Vector-Valued Kernel Ridge Regression for Complex-Valued Parametric Modeling of High-Speed Interconnects*.

– **IEEE Electronics Packaging Society Student Travel Grants**: Ethan Thieme, for the work titled *Transformed Gaussian Process Regression for Passivity-Aware Uncertainty Quantification*, and Yens Lindemans, for the work titled *Macromodeling of Electrically Long Structures Using a Delay-Aware Rational Szegő Kernel*.

In keeping with SPI tradition, the technical program was complemented by social events designed to highlight the architectural and cultural heritage of Turin. Three distinct experiences were organized to celebrate this 30th anniversary milestone:

– The Welcome Reception on Sunday, held at the magnificent Castello del Valentino, a royal residence and UNESCO World Heritage site, for everyone to catch up with familiar faces and network with new colleagues in a relaxed setting.

– The City Tour on Monday, a wonderful "royal" journey through Turin's historic center to discover the splendor of Italy's first capital. The day concluded in true Italian style with a delicious *pizzata* dinner, offering an informal atmosphere to unwind and socialize.

– The Gala Dinner on Tuesday, hosted at the spectacular *MAUTO - Museo Nazionale dell'Automobile*, was a memorable evening of fine dining and celebration, that beautifully reflected the workshop's own blend of tradition and forward-thinking innovation.

An event of this scale is only possible through collective dedication. We extend our deepest gratitude to the SPI Standing Committee for their continued stewardship, and to the Technical Program Committee for their rigorous review process, which resulted in a first-class technical program. A special acknowledgement as well to our keynote speaker and to the Global SIPI University instructors for their generous availability and for sharing their invaluable expertise with our community. Finally, our sincere appreciation goes also to our sponsoring IEEE societies, to our organizing hosts, and to our private sponsors, whose vital support fuels this workshop.

To all **SPI 2026** participants, your attendance and contributions are much appreciated and played an essential role in the resounding success of this landmark 30th anniversary occasion. We warmly thank you and sincerely hope the event fulfilled your expectations and provided inspiring and lasting memories.

Thank you for an outstanding **SPI 2026**! Join us again for the 2027 edition in **Riva del Garda, Italy**!

*Paolo Manfredi*, IEEE SPI 2026 Workshop Chair
*Tom Dhaene & Riccardo Trinchero*, IEEE SPI 2026 Program Co-Chairs
*Tommaso Bradde*, IEEE SPI 2026 Publication Chair

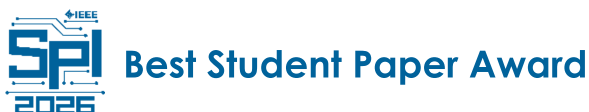
SPI 2026 Official Group Photo

Continuing the SPI workshop tradition of acknowledging remarkable research and scholarly contributions, as well as encouraging the next generation of leaders within the SPI community, we are proud to celebrate the recipients of the **SPI 2026 Awards & Grants**. Our warmest congratulations go to the winners for their outstanding papers and exceptional contributions to our field!

Tim Pattyn, Daniël De Zutter, Martijn Huynen, Dries Vande Ginste

*Ghent University - imec, Belgium*

**A Novel Vectorial Unified Transform for the Full-Wave Broadband Characterization of On-chip Passives**

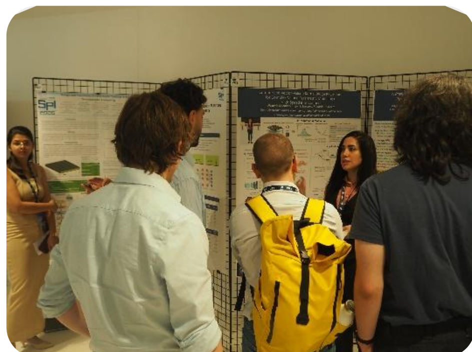


Atacan Tuhan, Damian Marek, Yongzhong Li, Piero Triverio

*University of Toronto, Canada*

**A Scalable Distributed Electromagnetic Solver for 3D Integrated Circuit Design**

## Best Poster Award



Nazanin Soleimani, Igor Simone Stievano, Riccardo Trinchero

*Politecnico di Torino, Italy*

**Compressed Vector-Valued Kernel Ridge Regression for Complex-Valued Parametric Modeling of High-Speed Interconnects**

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## Student Travel Grants

Ethan Thieme, Xu Chen

*University of Illinois Urbana-Champaign, USA*

**Transformed Gaussian Process Regression for Passivity-Aware Uncertainty Quantification**

Yens Lindemans, Thijs Ullrick, Ivo Couckuyt, Dirk Deschrijver, Tom Dhaene

*Ghent University – imec, Belgium*

**Macromodeling of Electrically Long Structures Using a Delay-Aware Rational Szegő Kernel**

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*Politecnico di Torino, Turin (ITA)*

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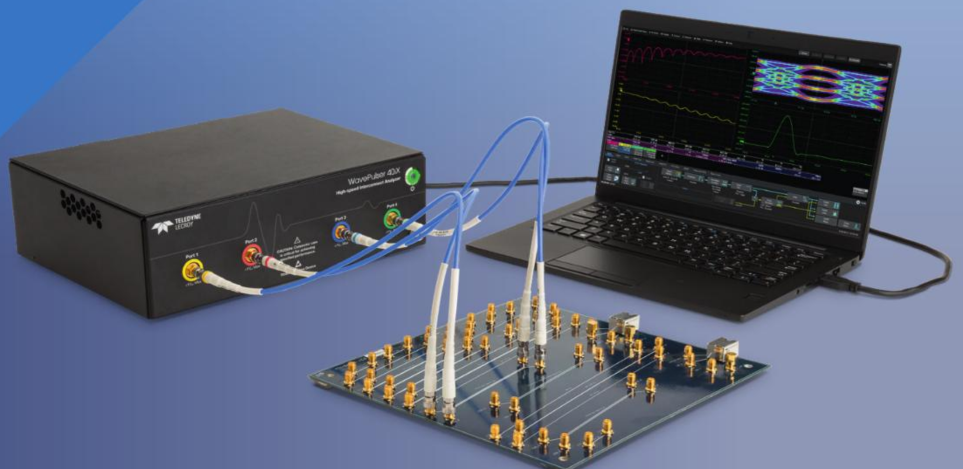

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# PROGRAM OVERVIEW

**June 14, Sunday – Castello del Valentino**

| Time | Event |
|---|---|
| 09:00-09:30 | On-Site Registration |
| 09:30-09:45 | **Welcome and Opening** |
| 09:45-10:30 | **Keynote** |
| 10:30-11:00 | Coffee Break / Networking |
| 11:00-11:45 | **Introduction to SI and PI** |
| 11:45-12:30 | **Signal Integrity I** |
| 12:30-14:00 | Lunch / Networking |
| 14:00-14:45 | **Signal Integrity II** |
| 14:45-15:30 | **Signal Integrity III** |
| 15:30-16:00 | Coffee Break / Networking |
| 16:00-16:45 | **Power Integrity** |
| 16:45-17:30 | **Application Perspective** |
| 18:00 onwards | **Welcome Reception** |

**June 15, Monday – Energy Center**

| Time | Event |
|---|---|
| 08:30-09:00 | On-Site Registration |
| 09:00-09:15 | **Opening Session** |
| 09:15-10:00 | **KEYNOTE** Breaking the AI Power Wall – An Overview of the Challenges and Solutions |
| 10:00-10:40 | **SESSION 1.1** ML/AI for Signal and Power Integrity |
| 10:40-11:10 | Coffee Break / Networking |
| 11:10-12:30 | **SESSION 1.2** ML/AI for Signal and Power Integrity |
| 12:30-14:00 | Lunch / Networking |
| 14:00-15:20 | **SESSION 2** Computational Electromagnetics |
| 15:20-16:00 | **Sponsors' Tech Pitches** |
| 16:00-17:00 | **POSTER SESSION** & Coffee-Break |
| 18:15 onwards | **City Tour** |

**June 16, Tuesday – Energy Center**

| Time | Event |
|---|---|
| 08:30-09:30 | **SESSION 3** Surrogate Modeling and Machine Learning |
| 09:30-10:10 | **SESSION 4** 2.5D/3D Networks for High-Performance Applications |
| 10:10-10:40 | Coffee Break / Networking |
| 10:40-12:00 | **SPECIAL SESSION** History of SPI – 30th Anniversary |
| 12:00-13:30 | Lunch / Networking |
| 13:30-15:10 | **SESSION 5** Crosstalk and EMC |
| 15:10-15:40 | Coffee Break / Networking |
| 15:40-16:40 | **SESSION 6** High-Speed Signal Integrity |
| 16:40-16:50 | **Activity IEEE EDMS-TC** |
| 18:15 onwards | **Gala Dinner** |

**June 17, Wednesday – Energy Center**

| Time | Event |
|---|---|
| 09:00-10:40 | **SESSION 7** Advanced Design for Signal Integrity and Packaging |
| 10:40-11:10 | Coffee Break / Networking |
| 11:10-12:30 | **SESSION 8** Macromodeling and Model Order Reduction |
| 12:30-12:40 | **Closing Session** |
| 12:40-14:00 | Lunch / Networking |
| 14:00-18:00 | **European Hybrid IBIS Summit** |

# June 14, Sunday

## Global SIPI University & Welcome Reception @ Castello del Valentino

### Global Signal Integrity and Power Integrity (SIPI) University

The **Global Signal Integrity and Power Integrity (SIPI) University** was successfully introduced by the IEEE EMC Society at the EMC+SIPI 2024 in Phoenix, AZ, USA, and, following high demand, held for a second time at the EMC+SIPI 2025 in Raleigh, NC, USA. Continuing its tradition of excellence, the program will once again offer its comprehensive two-day curriculum at the 2026 IEEE International Symposium on EMC+SIPI in Dallas, TX, USA.

In a spirit of close collaboration and advancing technology worldwide, the IEEE EMC Society, in partnership with the IEEE EPS and the SPI 2026 Organization, inaugurated the **Global SIPI University** at the **2026 IEEE Workshop on Signal and Power Integrity (SPI)**, held in Turin, Italy, bringing this premier educational experience to a wider international audience and ensuring another year of intensive, top-quality learning across both continents.

**Course Overview**

Modern high-speed digital systems are rapidly increasing in complexity as data rates climb and power distribution demands intensify. These unprecedented challenges require dedicated expertise in Signal Integrity (SI) and Power Integrity (PI), skills that are critically sought after by industry but are often scarce in traditional academic programs.

The Global SIPI University @ SPI 2026 was a focused, one-day intensive course, outlined to equip students, technicians, and engineers with further tools to bridge this crucial skills gap. Attendees dived deep into SI and PI core concepts, learning directly from experienced and renowned instructors drawn from both industry and academia. The carefully curated curriculum aimed to balance fundamental theory with direct practical application, covering analytical methods, simulation tools, and measurement techniques for solution validation.

| 09:00 - 09:30 | On-Site Registration |
|---|---|

## Castello del Valentino

Google Maps: Viale Pier Andrea Mattioli 39, 10125 Torino

## 09:30 - 09:45 Welcome and Opening

**Francesco de Paulis**

*University of L'Aquila, L'Aquila, Italy*

Francesco de Paulis (IEEE Senior Member) received the M.S. degree in Electrical Engineering in May 2008 from Missouri University of Science and Technology (formerly University of Missouri-Rolla), USA, and the PhD degree in Electrical and Information Engineering in 2012 from the University of L'Aquila, Italy. He is currently an Associate Professor at the Electromagnetic Compatibility and Signal Integrity Laboratory, University of L'Aquila, and an Adjunct Professor at the Missouri University of Science and Technology. He serves as Guest Editor for the IEEE Transactions on Signal and Power Integrity and as Associate Editor for the IEEE Transactions on Instrumentation and Measurements. He is a member of the Board of Governors of the IEEE EMC Society (2025-2027). His main research interests are in signal and power integrity, high speed channel design, electromagnetic compatibility, antenna design and measurement techniques.

**Christian Schuster**

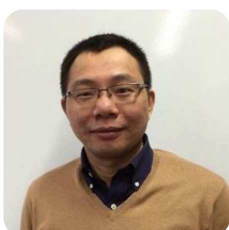
*Hamburg University of Technology, Hamburg, Germany*

Christian Schuster (IEEE Fellow) received a Diploma degree in physics in 1996 and a Ph.D. degree in electrical engineering in 2000. Since 2006 he is a full professor at Hamburg University of Technology (TUHH), Germany. Prior to TUHH he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA. His interests include signal and power integrity of digital systems, multiport measurement and calibration techniques, and development of physics-based as well as data-based modeling, simulation and optimization methods for EMC+SIPI. In the recent past, he has served as an Associate Editor for the IEEE Transactions on EMC, as an Adjunct Associate Professor at the School of Electrical and Computer Engineering of the Georgia Institute of Technology, and as the President of the NIT Northern School of Technology Management at TUHH.

## 09:45 - 10:30 Keynote

### SI and PI challenges for enterprise server design

In recent years, enterprise server deployment growth is exponential, fueled by AI acceleration, cloud-native computing, and heterogeneous workloads. These systems now demand extreme bandwidth densities and power delivery capabilities, often exceeding multi-terabit signaling and multi-kilowatt power envelopes. Such requirements place profound challenges in signal integrity (SI) and power integrity (PI) design. This keynote will examine the SI and PI challenges inherent to modern server design, with emphasis on high-speed interconnects, advanced packaging technologies, and power delivery networks. In particular, this talk will show how physical constraints such as board real estate, mechanical limits, and cost-performance trade-offs influence design decisions. It will include practical cases, highlighting co-design strategies, modeling techniques, and system-level optimization approaches. The goal is to foster a deeper understanding of how SI/PI methodologies evolve to meet the demands of next-generation computing infrastructure.



**Xiaomin Duan**

*IBM Research and Development GmbH, Ehningen, Germany*

Xiaomin Duan (IEEE Senior Member) is currently technical lead responsible for IBM Z processor packaging design and integration. He received the M.S. degree in microelectronics and microsystems and the Ph.D. degree in electrical engineering from the Hamburg University of Technology, Hamburg,

Germany, in 2007 and 2012, respectively. He was a Post-Doctoral Researcher with the Institute of Electromagnetic Theory, Technical University of Hamburg, from 2012 to 2013, and the RF and High Speed Group, Fraunhofer Institute for Reliability and Microintegration, Berlin, Germany, from 2013 to 2015. Since 2016, he has been with IBM Germany Research & Development GmbH, Germany.

| 10:30 - 11:00 | Coffee Break / Networking |
|---|---|

| **11:00 - 11:45** | **Introduction to SI and PI** |
|---|---|

## Evolution from the basics to the current technology

This presentation will introduce the concepts of signal and power integrity, and the evolution, in the past two decades, of the challenges associated with the modeling, analysis, and design of high speed interconnects and high-current PDNs. An overview of the current trends based on the state of the art of the technology discussed in the following sessions will be given.

**Francesco de Paulis**

*University of L'Aquila, L'Aquila, Italy*

Francesco de Paulis (IEEE Senior Member) received the M.S. degree in Electrical Engineering in May 2008 from Missouri University of Science and Technology (formerly University of Missouri-Rolla), USA, and the PhD degree in Electrical and Information Engineering in 2012 from the University of L'Aquila, Italy. He is currently an Associate Professor at the Electromagnetic Compatibility and Signal Integrity Laboratory, University of L'Aquila, and an Adjunct Professor at the Missouri University of Science and Technology. He serves as Guest Editor for the IEEE Transactions on Signal and Power Integrity and as Associate Editor for the IEEE Transactions on Instrumentation and Measurements. He is a member of the Board of Governors of the IEEE EMC Society (2025-2027). His main research interests are in signal and power integrity, high speed channel design, electromagnetic compatibility, antenna design and measurement techniques.

| **11:45 - 12:30** | **Signal Integrity I** |
|---|---|

## Lumped vs. distributed discontinuities, transmission line effects, crosstalk and losses

As data rates and edge speeds in modern electronic systems continue to rise, the distinction between lumped and distributed discontinuities becomes critical for accurate signal-integrity and electromagnetic-compatibility design. This presentation gives an overview of how geometric and material transitions within interconnects behave either as localized impedance discontinuities or as electrically long structures exhibiting full transmission-line effects. Key mechanisms – including reflections, standing waves, and frequency-dependent propagation – are discussed to illustrate when traditional lumped-element approximations break down. The study further examines how distributed coupling paths give rise to near-end and far-end crosstalk, emphasizing the impact of trace geometry, dielectric properties, and return-path configuration. Additionally, conductor and dielectric losses are discussed in the context of attenuation, phase distortion, and their influence on high-speed waveform integrity. By integrating these phenomena into a unified perspective, the presentation highlights practical

design considerations for minimizing signal degradation and ensuring robust performance across high-frequency interconnects.

**Andreas Hardock**

*Nexperia Germany GmbH, Hamburg, Germany*

Andreas Hardock (IEEE Senior Member) studied nanostructure technology at the Julius Maximilian University of Würzburg and did his PhD in the field of functional vias at the Technical University of Hamburg-Harburg. He began his professional career in 2015 in the automotive industry as an EMC engineer at Behr-Hella Thermocontrol. From 2016 to 2020, he worked at Continental Automotive GmbH in Babenhausen, serving as a hardware architect responsible for SI/PI, EMC, and ESD topics in product development. In 2020, Andreas joined Nexperia in the group of Product Application, focusing on ESD and EMC technologies and products for the automotive sector. He is a Senior Member of the IEEE and has been part of the EMC Society since 2011. Since 2019, he has been an active contributor to the IEEE German EMC Chapter.

| 12:30 - 14:00 | Lunch / Networking |
|---|---|

| **14:00 - 14:45** | **Signal Integrity II** |
|---|---|

## 3D modeling and simulation, circuit modeling and simulation, equalization

3D electromagnetic modeling and simulation, circuit-level modeling and simulation, and equalization are foundational to modern electronic system design, particularly for high-speed and high-frequency applications. When applied in an integrated manner, these techniques enable accurate performance prediction, early identification of signal- and power-integrity challenges, and systematic design optimization prior to physical prototyping – significantly reducing development time, cost, and overall technical risk. This presentation will highlight the successful design of modern SoCs and ASICs for wearable devices and infrastructure systems supporting AI workloads. As these designs incorporate both in-package and external memories with high-speed I/O interfaces and therefore require comprehensive electromagnetic analysis and circuit-level simulation. The discussion will include detailed system-level modeling and analysis methodologies used to optimize end-to-end performance across the complete signal and power delivery paths.

**Wendem Beyene**

*Meta Platforms, Sunnyvale CA, USA*

Wendem Beyene (IEEE Fellow) is an Analog and Mixed-Signal Architect at Meta Platforms. He previously held technical and leadership roles at IBM, Hewlett-Packard, Agilent Technologies, Rambus, and Intel. He serves as a Senior Area Editor for the IEEE Transactions on CPMT. He has been a Distinguished Lecturer for the IEEE EPS society since 2020 and served for the IEEE EMC society in the past. Dr. Beyene has taught university-level courses in signal and power integrity and computer methods for circuit analysis and design. He has also served as General Chair for several IEEE conferences and is an Associate Fellow of the Ethiopian Academy of Sciences. Since 2022, he has organized the annual IEEE EPS– and EDS–sponsored DTMES conference in Addis Ababa, Ethiopia.

**14:45 - 15:30** **Signal Integrity III**

## VNA measurements in signal integrity

Signal integrity has become a critical aspect of modern high-speed digital design, today more than ever as data rates continue to rise and reliable transmission become essential. In this seminar, we will understand how VNAs are used to identify potential signal integrity issues and address them using tools and applications integrated in the network analyzer. First, we will cover the basics of VNA parameters and time domain analysis, which is necessary to gain the correct insights about my DUT. Then we will discuss the topic of de-embedding and see how it can help the designer make the correct choices when developing his PCB. We will end this presentation with a live demo of our VNA in action, including real measurements of transmission lines.

**Giordano Mariani**

*Rohde & Schwarz, Milan, Italy*

Giordano Mariani received the M.S. degree in Electrical Engineering from La Sapienza University in Rome in 2018. In the same year he joined a startup in the Netherlands, working on integrated photonics and specializing in RF testing, design and simulation. In 2022 he joined Rohde & Schwarz Italy as an application engineer. He focuses on applications for the Aerospace and Defense market, such as satellite testing, GNSS and RF component characterization. He has a strong background in VNA measurements and characterization of PCBs and transmission lines from a signal integrity perspective.

15:30 - 16:00 Coffee Break / Networking

**16:00 - 16:45** **Power Integrity**

## SoC on-die power integrity basics

Modern System-on-Chip (SoC) designs are highly optimised to accommodate an increasing number of transistors and components within the smallest possible feature size. To ensure robustness and reliability, these advanced implementations require precise pre-silicon analysis methodologies. Power Integrity is the discipline that studies the quality of Power Delivery Networks (PDNs), ensuring that Power/Ground connections for each transistor of an SoC meet specific design targets that guarantee functionality. This presentation will provide an overview of the concepts and general principles of SoC On-Die Power Integrity simulations for a generic digital SoC. The talk will also provide insights on SoC Physical Design, Power Grid implementation, SoC Power calculation and its optimization.

**Gianni Signorini**

*Apple, Munich, Germany*

Gianni Signorini holds a B.Sc. and M.Sc. (with honours) in Electronics Engineering from the University of Pisa, Italy, and a Ph.D. degree in Information Engineering from the same institution. From 2011 to 2018, he was with Intel Corporation (Munich, Germany) where he conducted research on Signal and Power Integrity co-simulations and methodology development in collaboration with the Department of

Electronics and Telecommunications (DET) at Politecnico di Torino, Italy. Since 2019, Gianni Signorini has been with Apple (Munich, Germany) where he leads an international team that is responsible for Power Integrity simulations of several Apple SoCs. Gianni Signorini was the recipient of 2015 IEEE SPI Best Student Paper Award. He has published several articles in IEEE journals and international conferences.

**16:45 - 17:30** **Application Perspective**

## SI and PI aware design of automotive interconnects

The necessity of further improved EMC/ESD/SIPI behavior and optimized PCB design is obvious, because high-complexity products with enhanced safety/security requirements need to be managed. Advanced PCB's with BGA-IC packages, high-speed clock lines with rich spectral-content, high-frequency signals with sharp rise-times and high slew-rates, often require an increased number of stacked PCB layers. To benefit from leading-edge technology processes and functions, many IC's require several voltage-rails and an optimized PDN, allowing reliable Inter-Chip connections along with proper communication between Electrical Control Units. This presentation provides an overview of most current challenges and gives an outlook how the complexity and the challenges can be managed, while meeting cost and time to market constraints under the harsh conditions of automotive applications.

**Aman Gupta**

*NXP Semiconductors GmbH, Hamburg, Germany*

Aman Gupta was born in Raniganj, India. He received the MTech. degree in Microelectronics from BITS Pilani, Rajasthan, India, in 2023. In 2019, he joined Bosch Global Software Technologies, Bengaluru, India, where he was working as a Senior EMC Engineer. In 2023, he joined Valeo, Bietigheim-Bissingen, Germany, as an EMC Design Engineer and is currently working with NXP Semiconductors, Hamburg, Germany, as an EMC Engineer. He has authored in three technical papers, which includes one Journal on Antenna Design. His recent research interests include antenna design, electromagnetic interference/EMC, wireless communication.

**18:00 onwards** **Welcome Reception**

The Welcome Reception that took place at the magnificent Castello del Valentino offered an amazing setting to catch up with old colleagues, meet new peers, and forge new professional bonds, all while enjoying delicious appetizers and refreshing drinks to end the day on a more relaxed note!

# June 15, Monday

## Featured and Technical Sessions & Sponsors Exhibition @ Energy Center

Welcome to the core technical program of **SPI 2026 – 30th IEEE Workshop on Signal and Power Integrity**. This year's outstanding technical lineup brought together some of the brightest minds from academia and industry to tackle the most pressing challenges in the field – an invitation to attendees to immerse themselves in rigorous technical sessions, engage in premium networking events, and spark new collaborations that will contribute to shape the future of the SPI community.

**Sponsors Exhibition & Tech Pitches**

Innovation thrives on the synergy between research and commercial application. Attendees were invited to explore the Sponsors Exhibition and attend the scheduled Tech Pitches – a premier platform to discover the advanced tools and solutions shaping the industry today, engage directly with dedicated corporate experts, and gain valuable insights into pioneering technologies from the leading companies supporting SPI.

| 08:30 - 09:00 | On-Site Registration |
|---|---|

## Energy Center

Google Maps: Via Paolo Borsellino 38/16, 10138 Torino

| **09:00 - 09:15** | **Opening Session** |
|---|---|

**Paolo Manfredi**

*Politecnico di Torino, Turin, Italy*

Paolo Manfredi (IEEE Senior Member) received the M.Sc. degree in electronic engineering and the Ph.D. degree in information and communication technology from the Politecnico di Torino, Italy, in 2009 and 2013, respectively. He is currently a Full Professor with the EMC Group, Department of Electronics and Telecommunications, Politecnico di Torino. His research interests include several aspects of the modeling and simulation of circuits and transmission lines, with emphasis on uncertainty quantification, surrogate modeling, and machine learning. He serves as an Associate Editor for IEEE Journal on Multiscale and Multiphysics Computational Techniques and as Co-Chair of the Electrical Design, Modeling and Simulation Technical Committee of the IEEE Electronics Packaging Society.

**09:15 - 10:00** **KEYNOTE**

## Breaking the AI Power Wall – An Overview of the Challenges and Solutions

AI datacenters are facing a new class of Power Delivery (PD) and Power Integrity (PI) constraints driven by rapid scaling in GPU power and workload dynamics. As GPU power levels approach multiple kW, traditional MBVR based power delivery solutions become highly inefficient. It is estimated that less than half of the power that is fed to the racks will be used for compute. The rest is dissipated in the form of conversion losses, I2R losses and droop induced losses. In this talk we will take a closer look at the key PD/PI challenges in this segment as well as some novel solutions that are being developed to address these challenges.

**Kaladhar Radhakrishnan**

*Intel Corporation, Chandler AZ, USA*

Kaladhar Radhakrishnan is an Intel Fellow and a Power Delivery Architect with the Technology Development group at Intel. He has played a significant role in shaping and driving power delivery technologies for Intel microprocessors. His areas of expertise are in integrated voltage regulators, advanced packaging and passives technologies. Kaladhar is a two-time recipient of the Intel Achievement Award. He has authored 4 book chapters, over 50 technical papers in peer reviewed journals, and has been awarded 50 US patents. Kaladhar joined Intel in 2000 after he received his Ph.D. in Electrical Engineering from the University of Illinois at Urbana-Champaign, USA.

**10:00 - 10:40**

**SESSION 1.1**

**ML/AI for Signal and Power Integrity**

Chairs: Domenico Spina & Xu Chen

### 10:00

Sohrab Sheikh Sofla, Madhavan Swaminathan

*Pennsylvania State University, USA*

**Temperature-Aware ML Surrogates for Fast Signal-Integrity Prediction in Co-Packaged Optics**

### 10:20

Soumyadeep Chatterjee (1), Priyank Kashyap (2), Nirjhor Rouf (1), Chris Cheng (2), Paul Franzon (1)

*(1) North Carolina State University, USA; (2) Hewlett Packard Enterprise, USA*

**Modeling High-Speed SerDes Links with Symbolic Regression**

10:40 - 11:10 Coffee Break / Networking

**11:10 - 12:30** **SESSION 1.2**
**ML/AI for Signal and Power Integrity**
Chairs: Domenico Spina & Xu Chen

**11:10**
Tommy Weber, Til Hillebrecht, Christian Schuster
*Hamburg University of Technology, Germany*
**Using Decision Trees for Fast Error Identification in Physics-Based Modeling of PCB Structures**

**11:30** **IEEE EPS Student Travel Grant**
Yens Lindemans, Thijs Ullrick, Ivo Couckuyt, Dirk Deschrijver, Tom Dhaene
*Ghent University – imec, Belgium*
**Macromodeling of Electrically Long Structures Using a Delay-Aware Rational Szegő Kernel**

**11:50** **IEEE EPS Student Travel Grant**
Ethan Thieme, Xu Chen
*University of Illinois Urbana-Champaign, USA*
**Transformed Gaussian Process Regression for Passivity-Aware Uncertainty Quantification**

**12:10**
Aakanksha Verma, Dyuti Basu, Avirup Dasgupta, Sourajeet Roy
*Indian Institute of Technology Roorkee, India*
**Efficient Stochastic Modeling of Distributed Transmission Line Networks using Homotopy Assisted Physics Informed Neural Networks**

12:30 - 14:00 Lunch / Networking

**14:00 - 15:20** **SESSION 2**
**Computational Electromagnetics**
Chairs: Piero Triverio & Dries Vande Ginste

**14:00**
Yongzhong Li, Piero Triverio
*University of Toronto, Canada*
**A Comparative Study of Acceleration Algorithms for Integral Equation Methods**

**14:20**

Atacan Tuhan, Damian Marek, Yongzhong Li, Piero Triverio
*University of Toronto, Canada*
**A Scalable Distributed Electromagnetic Solver for 3D Integrated Circuit Design**

**14:40**

Tim Pattyn, Daniël De Zutter, Martijn Huynen, Dries Vande Ginste
*Ghent University - imec, Belgium*
**A Novel Vectorial Unified Transform for the Full-Wave Broadband Characterization of On-chip Passives**

**15:00**
Madhavan Swaminathan (1), Yiliang Guo (2), Yifan Wang (2)
*(1) Pennsylvania State University, USA; (2) Georgia Institute of Technology, USA*
**Accelerated Electromagnetic Simulation Using the Laguerre-FDTD Method and Machine Learning**

**15:20 - 16:00** **SPONSORS' TECH PITCHES**
Chair: Paolo Manfredi

**15:20**
***Huawei Technologies*** – Marco De Stefano

**15:30**
***Siemens EDA*** – Carlo Bleu

**15:40**
***STMicroelectronics*** – Davide Lena

**15:50**
***Zuken*** – Ralf Bruening

**16:00 - 17:00** **POSTER SESSION** & Coffee Break
Chairs: Thomas Kühler & Antonio Maffucci

**P01**
Raushan Kumar (1), Manish Bansal (1), Davide Lena (2), Marcello Cicchetti (2)
*(1) STMicroelectronics Pvt Ltd., India; (2) STMicroelectronics Pvt Ltd., Italy*
**Accurate SI/PI Analysis of Differential Interfaces: Addressing Limitations in Power Aware IBIS Modeling Methodology**

**P02**
Alexandre Plot (1), Benoît Goral (1), Béatrice Azanowsky (1), Philippe Besnier (2)
*(1) Thales SIX GTS, France; (2) Univ Rennes, CNRS, IETR, France*
**Designing for Board Level Electromagnetic Compatibility Through a Systematic Learning Methodology**

**P03**

Til Hillebrecht (1), Johannes Alfert (1), Pantelis Lelekas (2), Nikolaos Sismanis (2), Georgios Bouzianas (2), Christian Schuster (1)
*(1) Hamburg University of Technology, Germany; (2) Altair Engineering MEPE, Greece*

**Modeling and Improving Transmission of High-Speed Vias on PCBs up to 200 GHz**

**P04**

Gia Ngoc Phung (1), Thomas Flisgen (2), Gregor Streitenberger (1), Abhijeet Kanitkar (3), Uwe Arz (1), Wolfgang Heinrich (3)
*(1) Physikalisch-Technische Bundesanstalt, Germany; (2) BTU Cottbus-Senftenberg, Germany; (3) Ferdinand-Braun-Institut, Germany*

**A Comparative Study of Microstrip Line Models up to 500 GHz**

**P05**

Kaisheng Hu
*Ciena, Canada*

**Measurement-Calibrated PCB Material Modeling for Millimeter-Wave Signal Integrity**

**P06**

Tommaso Cappello
*Villanova University, USA*

**Low-Latency High-Speed RF Transmitters with Analog Pre-Distortion Power Amplifiers**

**P07**

Twinkel Manna (1), Gulafsha Bhatti (2), Aakanksha Verma (3), Sourajeet Roy (3), Yash Agrawal (2), Rohit Sharma (1)
*(1) Indian Institute of Technology Ropar, India; (2) Dhirubhai Ambani University, India; (3) Indian Institute of Technology Roorkee, India*

**Design and Simulation of Stretchable Crossbar Array for Neuromorphic Computing**

**P08**

Mohamed Kheir (1), Henning Mextorf (2)
*(1) University of Southern Denmark, Denmark; (2) West Coast University of Applied Sciences, Germany*

**ML-Based Surrogate Modeling of Capacitance Matrices in Multiconductor PCB Interconnects**

**P09**

Nazanin Soleimani, Igor Simone Stievano, Riccardo Trinchero
*Politecnico di Torino, Italy*

**Compressed Vector-Valued Kernel Ridge Regression for Complex-Valued Parametric Modeling of High-Speed Interconnects**

**P10**

Dilyorjon Yuldashev (1), Marco Atlante (1,2), Igor Simone Stievano (1), Riccardo Trinchero (1)
*(1) Politecnico di Torino, Italy; (2) Univ Brest, Lab-STICC, CNRS, France*

**A Preliminary Study on Kernel Ridge Regression for Parametric Behavioral Modeling of IC Buffers**

**P11**

Haiyue Yuan (1,2), Tao Wei (1), Yuhao Huang (1), Yajun Lv (1), Jun Wang (1), Feng Wu (1), Xiuqin Chu (1)
*(1) Xidian University, China; (2) Politecnico di Torino, Italy*

**Fast Calculation of Probability Distribution of Voltage Noise Based on Parameter Estimation**

**P12**

Xiao Chen, Gang Zhang, Jinghao Su
*Harbin Institute of Technology, China*

**A Two-dimensional Partial Element-Based Formulation for the Per-unit-length Parameter Calculation of Conductors**

**P13**

Hongyang Liu, Tejas Kulkarni, Ganesh Subbarayan, Cheng-Kok Koh, Dan Jiao
*Purdue University, USA*

**Full-Scale GPU-Accelerated Transient EM-Thermal-Mechanical Co-Simulation for Early-Stage Design of Advanced Packages**

**P14**

Si-Ping Gao (1,2), Jiahong Chen (1), Francesco de Paulis (3), En-Xiao Liu (4), Wenjian Yu (5)
*(1) Nanjing University of Aeronautics and Astronautics, China; (2) Beijing National Research Center for Information Science and Technology, China; (3) University of L'Aquila, Italy; (4) A*STAR IHPC, Singapore; (5) Tsinghua University, China*

**Equivalent Circuit Modeling of Aperiodic On-Silicon PDNs for Fast What-If Analysis**

**18:15 onwards** **City Tour**

Our attendees embarked on a "royal" journey through Turin's historic heart to uncover more than two millennia of history spanning from Roman origins to Baroque splendor. This exclusive guided tour was a wonderful opportunity to admire majestic squares and UNESCO World Heritage highlights that showcased the grandeur of Italy's first capital. The day ended in true Italian style with a delicious *pizzata* dinner, for everyone to unwind and share a laugh together!

# June 16, Tuesday

**Featured and Technical Sessions & Sponsors Exhibition @ Energy Center**

## SESSION 3
**08:30 - 09:30** **Surrogate Modeling and Machine Learning**

Chairs: Ramachandra Achar & Flavio Canavero

**08:30**

Simon Nau (1), Jan Krummenauer (1), Shaif Saleem (1), André Zimmermann (2)
*(1) Robert Bosch GmbH, Germany; (2) University of Stuttgart, Germany*

**Comparison of Tree Search and Reinforcement Learning Methods for Macromodel Synthesis**

**08:50**

Tse-Jui Huang, Tzong-Lin Wu
*National Taiwan University, Taiwan*

**A Physics-Informed 1D-CNN Surrogate Model Using Geometric Features for Mode Conversion Prediction in High-Density C-PHY Routing**

**09:10**

Ahsan Javaid, Ramachandra Achar
*Carleton University, Canada*

**Transformer-based Deep Equilibrium Model for Interconnects with Large Number of Coupled Lines**

## SESSION 4
**09:30 - 10:10** **2.5D/3D Networks for High-Performance Applications**

Chairs: Inna Partin-Vaisband & Madhavan Swaminathan

**09:30**

Andres Ayes, Eby G. Friedman
*University of Rochester, USA*

**Power Integrity in 3-D Chiplet Systems with Intermediate Layers**

**09:50**

Sriharini Krishnakumar, Inna Partin-Vaisband
*University of Illinois Chicago, USA*

**Power-Integrity Modeling of VR Faults in High-Performance Applications**

| 10:10 - 10:40 | Coffee Break / Networking |
|---|---|

## 10:40 - 12:00 SPECIAL SESSION
## History of SPI – 30th Anniversary
Moderator: Stefano Grivet Talocia

This special session celebrated the 30th anniversary of SPI, highlighting the challenges and achievements that forged and continue to sustain the workshop's enduring success. Technical progress was reviewed and discussed, bridging the past, present, and future through facts and testimonials from a panel of distinguished speakers, current and former members of the SPI Standing Committee. Alongside historical retrospectives and technical insights, the session featured also a well-deserved tribute to workshop pioneer Prof. Flavio Canavero, on the occasion of his retirement, and an obituary honoring the memory of the late Prof. Elmar Griese, a long-time member of the SPI Technical Program Committee.

**Flavio Canavero**
*Politecnico di Torino, Italy*

**Michel Nakhla**
*Carleton University, Canada*

**José Schutt-Ainé**
*University of Illinois Urbana-Champaign, USA*

**Madhavan Swaminathan**
*Pennsylvania State University, USA*

**Antonio Maffucci**
*University of Cassino and Southern Lazio, Italy*

**Mihai Telescu**
*University of Brest, France*

**Dries Vande Ginste**
*Ghent University, Belgium*

**Stefano Grivet Talocia**
*Politecnico di Torino, Italy*

- **Introduction** – Stefano Grivet-Talocia
- **SPI Memories** – Flavio Canavero
- **SPI Perspective: A Brief History of SI/PI** – José Schutt-Ainé
- **Signaling and Power Distribution Challenges for 3D Heterogeneous Integration** – Madhavan Swaminathan
- **30 Years of Macromodeling @ SPI** – Stefano Grivet-Talocia
- **A Few Thoughts on the French Editions of SPI** – Mihai Telescu
- **Uncertainty Quantification at SPI** – Dries Vande Ginste
- **SPI Then and Now** – Michel Nakhla
- **Obituary: Elmar Griese** – Thomas Kühler *(University of Siegen, Germany)*
- **SPI at 30: Thirty Years of Interconnect Evolution** – Antonio Maffucci

| 12:00 - 13:30 | Lunch / Networking |
|---|---|

**13:30 - 15:10**

## SESSION 5
## Crosstalk and EMC
Chairs: Christian Schuster & Philippe Besnier

**13:30**
Yutaka Uematsu (1), Kentaro Jumonji (2)
*(1) Hitachi, Ltd., Japan; (2) Astemo, Ltd., Japan*
**A Shield-Assisted Dual-Side Common-Mode Choke Coils Architecture for Compact Automotive Ethernet ECUs**

**13:50**
Han-Ting Lin, Andreas Weisshaar
*Oregon State University, USA*
**A Compact 8–18 GHz 150-ps True-Time-Delay Line in 0.18 µm SiGe BiCMOS**

**14:10**
Min Kim, Shilong Zhang, Geuna Chang, Youngsoo Shin
*Korea Advanced Institute of Science and Technology, South Korea*
**Signal-Integrity-Aware Routing and Shielding for UCIe-Compliant 2.5D ICs**

**14:30**

Jose Enrique Hernandez-Bonilla (1), Torben Wendt (1), Torsten Reuschel (2), Cheng Yang (3), Christian Schuster (3)

*(1) Robert Bosch GmbH, Germany; (2) University of New Brunswick, Canada; (3) Hamburg University of Technology, Germany*

**Behavior of Crosstalk in Environmentally-Impacted Automotive PCB Interconnects and Effect on Signal Transmission**

**14:50**

Moritz Gappa (1), Burkhard Heinke (1), Cheng Yang (2), Christian Schuster (2)

*(1) Airbus Operations GmbH, Germany; (2) Hamburg University of Technology, Germany*

**Systematic and Fast Crosstalk Modeling of 10Base-T1S Data Links in the Aircraft Cabin**

| 15:10 - 15:40 | Coffee Break / Networking |
| --- | --- |

**15:40 - 16:50**

## SESSION 6
## High-speed Signal Integrity

Chairs: Francesco de Paulis & Xiaomin Duan

**15:40**

Davit Kharshiladze (1), Hyunwook Park (1), Zhiping Yang (2), Chulsoon Hwang (1)

*(1) Missouri University of Science and Technology, USA; (2) PCB Automation Inc., USA*

**Boosting High-speed Channel Transformer Performance with Gating Neural Network**

**16:00**

Mike Resso (1), Pratik Ghate (2), Tim Wang Lee (1), Rick Rabinovich (1)

*(1) Keysight Technologies, USA; (2) FormFactor, Inc., USA*

**Signal Integrity Microprobing Strategies for Managing Channel Loss and Dense Packaging in AI Infrastructure Interconnects**

**16:20**

Andrew Josephson (1), Francesco de Paulis (2)

*(1) Samtec, USA; (2) University of L'Aquila, Italy*

**Over-Moded Coaxial Test Cables for 425 Gbps PAM4 SerDes Validation Test Margin**

**16:40 - 16:50** **IEEE TC-EDMS**

Paolo Manfredi
*Politecnico di Torino, Italy*

**Activity of the IEEE Electrical Design, Modeling and Simulation technical committee**

**18:15 onwards** **Gala Dinner**

As the crown jewel of this year's social program, the Gala Dinner was an unforgettable evening driven by the innovative spirit of Turin. Hosted at the *MAUTO - Museo Nazionale dell'Automobile*, it was a shared special moment of fine dining and celebration – including the announcement of the **SPI 2026 Awards & Grants** winners – all in a spectacular environment that beautifully steered tradition into the future!

The Best Paper Award recognizes the foremost contribution among all papers submitted to the workshop. Finalists are shortlisted based on the review process results, with a dedicated jury selecting the winner based on technical excellence, novelty, and potential impact on the field. To be eligible, the paper must be presented live at the workshop.

The Best Student Paper Award recognizes excellence in research for papers primarily authored by a student. To be eligible, interested students must submit a formal application and the paper must be presented live at the workshop.

The Best Poster Award recognizes the most outstanding visual and technical presentation among all posters presented live at the workshop, taking into account research excellence alongside clear and engaging communication.

The IEEE Electronics Packaging Society is pleased to provide a special Travel Grant to two students presenting their work at the workshop. The Grants are intended to support the costs directly tied to the event's attendance, with reimbursements up to the limits of 1600 USD for students from European institutions and 2450 USD for students from non-European institutions.

# June 17, Wednesday

**Featured and Technical Sessions & Sponsors Exhibition @ Energy Center**

**09:00 - 10:40**

## SESSION 7
## Advanced Design for Signal Integrity and Packaging

Chairs: Grégory Houzet & Thierry Lacrevaz

**09:00**

Antonio Maffucci (1,2), Ciro D'Elia (1,2), Alfredo Babusci (3), Andrea Gaetano Chiariello (4)
*(1) University of Cassino and Southern Lazio, Italy; (2) EUT+ Institute of Nanomaterials and Nanotechnologies EUTINN, European Union; (3) Monozukuri spa, Italy; (4) University of Campania "L. Vanvitelli", Italy*

**Signal Integrity Analysis of Integrated THz Graphene Antennas**

**09:20**

Francesco Siconolfi (1), Daniele Pinchera (1), Luca Tari (1), Antonio Maffucci (1), Gabriele Cavaliere (2), Isaac Appiah Otoo (3), Maria Cojocari (3), Sarah Sibilia (4), Francesco Cristiano (5), Gaspare Giovinco (1)
*(1) University of Cassino and Southern Lazio, Italy; (2) University of Salerno, Italy; (3) University of Eastern Finland, Finland; (4) E-Lectra srl, Italy; (5) Nanesa srl, Italy*

**A Multifunctional Graphene Coating for Advanced Electronic Packaging**

**09:40**

Taeho Park (1,2), SoYoung Kim (1)
*(1) Sungkyunkwan University, South Korea; (2) Samsung Electronics Co., Ltd., South Korea*

**A Methodology for Minimizing Driver Usage in High-Speed On-Chip Interconnects in Pre-Layout Phase**

**10:00**

Shilong Zhang, Gyeongjin Kim, Youngsoo Shin
*Korea Advanced Institute of Science and Technology, South Korea*

**Fully Automated Thermal-Aware Trace Routing for Chip-on-Film Designs**

**10:20**

Gabriel Vaintrub (1), Grégory Houzet (1), Edouard Rochefeuille (1), David Auchere (2), Laurent Schwartz (2), Thierry Lacrevaz (1)
*(1) CROMA, CNRS, Univ. Savoie Mont-Blanc, France; (2) STMicroelectronics, France*

**Development of a method for extracting the permittivity and permeability of molding compounds for IC packaging using a trident waveguide**

10:40 - 11:10 Coffee Break / Networking

**11:10 - 12:30**

## SESSION 8
## Macromodeling and Model Order Reduction
Chairs: Roni Khazaka & Stefano Grivet Talocia

**11:10**
Bijan Shahriari, Roni Khazaka
*McGill University, Canada*
**HIPPO-GRU Circuit Macro-Models based on Time- and Frequency-Domain Data**

**11:30**
Rayeed Rahman Ananda, Ramachandra Achar
*Carleton University, Canada*
**GPU-Accelerated Structure-Preserving Model Order Reduction of Large Multi-Port RLC Interconnects**

**11:50**
Owen Czuchra, Dries Peumans, John Lataire, Domenico Spina
*Vrije Universiteit Brussel, Belgium*
**Automatic Model-Based Characterization For Filter Design Verification**

**12:10**
Tommaso Bradde, Stefano Grivet-Talocia
*Politecnico di Torino, Italy*
**On Building $\mathcal{D}$-Stable Macromodels**

**12:30 - 12:40** **Closing Session**

12:40 - 14:00 Lunch / Networking

**14:00 - 18:00**

## European Hybrid IBIS Summit
Chair: Ralf Bruening

Meeting Agenda available at spi-workshop.org/ibis-summit.

spi2026@polito.it spi-workshop.org ieee-spi-workshop ieee_spi_workshop

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### Administrative Secretariat

**Manuela Trinchero** – *SELENE s.r.l., Italy*

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**Matteo Berrettoni** – *Politecnico di Torino, Italy*
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**Valentina Rinaudo** – *Politecnico di Torino, Italy*

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JUNE 14-17
TURIN, ITALY

# 30th IEEE WORKSHOP ON SIGNAL AND POWER INTEGRITY