



## PRELIMINARY PROGRAM

June 14, Sunday Castello del Valentino		June 15, Monday Energy Center		June 16, Tuesday Energy Center		June 17, Wednesday Energy Center	
09:00-09:30	On-Site Registration G-SIPI-U	08:30-09:00	On-Site Registration SPI	08:30-09:30	<b>SESSION 3</b> Surrogate Modeling and Machine Learning	09:00-10:40	<b>SESSION 7</b> Advanced Design for Signal Integrity and Packaging
09:30-09:45	Opening	09:00-09:15	Opening Session	09:30-10:10	<b>SESSION 4</b> 2.5D/3D Networks for High-Performance Applications	10:40-11:10	Coffee Break / Networking
09:45-10:30	Keynote	09:15-10:00	<b>KEYNOTE</b> Breaking the AI Power Wall – An Overview of the Challenges and Solutions	10:10-10:40	Coffee Break / Networking	11:10-12:30	<b>SESSION 8</b> Macromodeling and Model Order Reduction
10:30-11:00	Coffee Break / Networking	10:00-10:40	<b>SESSION 1.1</b> ML/AI for Signal and Power Integrity	10:40-12:00	<b>SPECIAL SESSION</b> History of SPI – 30th Anniversary	12:30-12:40	Closing Session
11:00-11:45	Introduction to SI and PI	10:40-11:10	Coffee Break / Networking	12:00-13:30	Lunch / Networking	12:40-14:00	Lunch / Networking
11:45-12:30	Signal Integrity I	11:10-12:30	<b>SESSION 1.2</b> ML/AI for Signal and Power Integrity	13:30-15:10	<b>SESSION 5</b> Crosstalk and EMC	14:00-18:00	<b>IBIS Summit</b>
12:30-14:00	Lunch / Networking	12:30-14:00	Lunch / Networking	15:10-15:40	Coffee Break / Networking		
14:00-14:45	Signal Integrity II	14:00-15:20	<b>SESSION 2</b> Computational Electromagnetics	15:40-17:00	<b>SESSION 6</b> High-speed Signal Integrity		
14:45-15:30	Signal Integrity III	15:20-15:50	Sponsors' Tech Pitches				
15:30-16:00	Coffee Break / Networking	15:50-16:00	Activity IEEE EDMS-TC				
16:00-16:45	Power Integrity	16:00-17:00	<b>POSTER SESSION</b> & Coffee-Break				
16:45-17:30	Application Perspective						
18:00 onwards	Welcome Reception	18:15 onwards	City Tour	18:15 onwards	Gala Dinner		

# Global SIPI University

June 14, Sunday

Castello del Valentino

09:30 - 09:45

Opening

Francesco de Paulis (1), Christian Schuster (2)

(1) University of L'Aquila, Italy; (2) Hamburg University of Technology, Germany

09:45 - 10:30

Keynote

Xiaomin Duan

IBM Research and Development GmbH, Germany

**SI and PI challenges for enterprise server design**

11:00 - 11:45

Introduction to SI and PI

Francesco de Paulis

University of L'Aquila, Italy

**Evolution from the basics to the current technology**

11:45 - 12:30

Signal Integrity I

Andreas Hardock

Nexperia Germany GmbH, Hamburg, Germany

**Lumped vs. distributed discontinuities, transmission line effects, crosstalk and losses**

14:00 - 14:45

Signal Integrity II

Wendem Beyene

Meta Platforms, Sunnyvale CA, USA

**3D modeling and simulation, circuit modeling and simulation, equalization**

14:45 - 15:30

Signal Integrity III

Giordano Mariani

Rohde & Schwarz, Milan, Italy

**VNA measurements in signal integrity**

16:00 - 16:45

Power Integrity

Gianni Signorini

*Apple, Munich, Germany*

**SoC on-die power integrity basics**

16:45 - 17:30

Application Perspective

Peter Hank, Aman Gupta

*NXP Semiconductors GmbH, Hamburg, Germany*

**SI and PI aware design of automotive interconnects**

## SPI Featured and Technical Sessions

June 15, Monday

Energy Center

09:00 - 09:15

Opening Session

09:15 - 10:00

KEYNOTE

Kaladhar Radhakrishnan

*Intel Corporation, Chandler AZ, USA*

**Breaking the AI Power Wall – An Overview of the Challenges and Solutions**

SESSION 1.1

10:00 - 10:40

ML/AI for Signal and Power Integrity

10:00

Sohrab Sheikh Sofla, Madhavan Swaminathan

*Pennsylvania State University, USA*

**Temperature-Aware ML Surrogates for Fast Signal-Integrity Prediction in Co-Packaged Optics**

10:20

Soumyadeep Chatterjee (1), Priyank Kashyap (2), Nirjhor Rouf (1), Chris Cheng (2), Paul Franzon (1)  
*(1) North Carolina State University, USA; (2) Hewlett Packard Enterprise, USA*

**Modeling High-Speed SerDes Links with Symbolic Regression**

SESSION 1.2

11:10 - 12:30

ML/AI for Signal and Power Integrity

11:10

Tommy Weber, Til Hillebrecht, Christian Schuster  
*Hamburg University of Technology, Germany*

**Using Decision Trees for Fast Error Identification in Physics-Based Modeling of PCB Structures**

11:30

Yens Lindemans, Thijs Ullrick, Ivo Couckuyt, Dirk Deschrijver, Tom Dhaene  
*Ghent University – imec, Belgium*

**Macromodeling of Electrically Long Structures Using a Delay-Aware Rational Szegő Kernel**

11:50

Ethan Thieme, Xu Chen  
*University of Illinois Urbana-Champaign, USA*

**Transformed Gaussian Process Regression for Passivity-Aware Uncertainty Quantification**

12:10

Aakanksha Verma, Dyuti Basu, Avirup Dasgupta, Sourajeet Roy  
*Indian Institute of Technology Roorkee, India*

**Efficient Stochastic Modeling of Distributed Transmission Line Networks using Homotopy Assisted Physics Informed Neural Networks**

SESSION 2

14:00 - 15:20

Computational Electromagnetics

14:00

Yongzhong Li, Piero Triverio  
*University of Toronto, Canada*

**A Comparative Study of Acceleration Algorithms for Integral Equation Methods**

14:20

Atacan Tuhan, Damian Marek, Yongzhong Li, Piero Triverio  
*University of Toronto, Canada*

**A Scalable Distributed Electromagnetic Solver for 3D Integrated Circuit Design**

14:40

Tim Pattyn, Daniël De Zutter, Martijn Huynen, Dries Vande Ginste  
*Ghent University - imec, Belgium*

**A Novel Vectorial Unified Transform for the Full-Wave Broadband Characterization of On-chip Passives**

15:00

Madhavan Swaminathan (1), Yiliang Guo (2), Yifan Wang (2)  
*(1) Pennsylvania State University, USA; (2) Georgia Institute of Technology, USA*

**Accelerated Electromagnetic Simulation Using the Laguerre-FDTD Method and Machine Learning**

15:20 - 15:50

## SPONSORS' TECH PITCHES

15:20

Huawei

15:30

Siemens

15:40

STMicroelectronics

15:50 - 16:00

## IEEE TC-EDMS

Paolo Manfredi*Politecnico di Torino, Italy*

Activity of the IEEE Electrical Design, Modeling and Simulation technical committee

16:00 - 17:00

## POSTER SESSION

P01

Rashan Kumar (1), Manish Bansal (1), Davide Lena (2), Marcello Cicchetti (2)*(1) STMicroelectronics Pvt Ltd., India; (2) STMicroelectronics Pvt Ltd., Italy***Accurate SI/PI Analysis of Differential Interfaces: Addressing Limitations in Power Aware IBIS Modeling Methodology**

P02

Alexandre Plot (1), Benoît Goral (1), Béatrice Azanowsky (1), Philippe Besnier (2)*(1) Thales SIX GTS, France; (2) Univ Rennes, CNRS, IETR, France***Designing for Board Level Electromagnetic Compatibility Through a Systematic Learning Methodology**

P03

Til Hillebrecht (1), Johannes Alfert (1), Pantelis Lelekas (2), Nikolaos Sismanis (2), Georgios Bouzianas (2), Christian Schuster (1)*(1) Hamburg University of Technology, Germany; (2) Altair Engineering MEPE, Greece***Modeling and Improving Transmission of High-Speed Vias on PCBs up to 200 GHz**

P04

Gia Ngoc Phung (1), Thomas Flisgen (2), Gregor Streitenberger (1), Abhijeet Kanitkar (3), Uwe Arz (1), Wolfgang Heinrich (3)*(1) Physikalisch-Technische Bundesanstalt, Germany; (2) BTU Cottbus-Senftenberg, Germany; (3) Ferdinand-Braun-Institut, Germany***A Comparative Study of Microstrip Line Models up to 500 GHz**

P05

Kaisheng Hu*Ciena, Canada***Measurement-Calibrated PCB Material Modeling for Millimeter-Wave Signal Integrity**

**P06**

Tommaso Cappello

*Villanova University, USA*

**Low-Latency High-Speed RF Transmitters with Analog Pre-Distortion Power Amplifiers**

**P07**

Twinkel Manna (1), Gulafsha Bhatti (2), Aakanksha Verma (3), Sourajeet Roy (3), Yash Agrawal (2), Rohit Sharma (1)

*(1) Indian Institute of Technology Ropar, India; (2) Dhirubhai Ambani University, India; (3) Indian Institute of Technology Roorkee, India*

**Design and Simulation of Stretchable Crossbar Array for Neuromorphic Computing**

**P08**

Mohamed Kheir (1), Henning Mextorf (2)

*(1) University of Southern Denmark, Denmark; (2) West Coast University of Applied Sciences, Germany*

**ML-Based Surrogate Modeling of Capacitance Matrices in Multiconductor PCB Interconnects**

**P09**

Nazanin Soleimani, Igor Simone Stievano, Riccardo Trincherio

*Politecnico di Torino, Italy*

**Compressed Vector-Valued Kernel Ridge Regression for Complex-Valued Parametric Modeling of High-Speed Interconnects**

**P10**

Dilyorjon Yuldashev (1), Marco Atlante (1,2), Igor Simone Stievano (1), Riccardo Trincherio (1)

*(1) Politecnico di Torino, Italy; (2) Univ Brest, Lab-STICC, CNRS, France*

**A Preliminary Study on Kernel Ridge Regression for Parametric Behavioral Modeling of IC Buffers**

**P11**

Haiyue Yuan (1,2), Tao Wei (1), Yuhao Huang (1), Yajun Lv (1), Jun Wang (1), Feng Wu (1), Xiuqin Chu (1)

*(1) Xidian University, China; (2) Politecnico di Torino, Italy*

**Fast Calculation of Probability Distribution of Voltage Noise Based on Parameter Estimation**

**P12**

Xiao Chen, Gang Zhang, Jinghao Su

*Harbin Institute of Technology, China*

**A Two-dimensional Partial Element-Based Formulation for the Per-unit-length Parameter Calculation of Conductors**

**P13**

Hongyang Liu, Tejas Kulkarni, Ganesh Subbarayan, Cheng-Kok Koh, Dan Jiao

*Purdue University, USA*

**Full-Scale GPU-Accelerated Transient EM-Thermal-Mechanical Co-Simulation for Early-Stage Design of Advanced Packages**

June 16, Tuesday

Energy Center

SESSION 3

08:30 - 09:30

Surrogate Modeling and Machine Learning

08:30

Simon Nau (1), Jan Krummenauer (1), Shaif Saleem (1), André Zimmermann (2)

(1) Robert Bosch GmbH, Germany; (2) University of Stuttgart, Germany

Comparison of Tree Search and Reinforcement Learning Methods for Macromodel Synthesis

08:50

Tse-Jui Huang, Tzong-Lin Wu

National Taiwan University, Taiwan

A Physics-Informed 1D-CNN Surrogate Model Using Geometric Features for Mode Conversion Prediction in High-Density C-PHY Routing

09:10

Ahsan Javaid, Ramachandra Achar

Carleton University, Canada

Transformer-based Deep Equilibrium Model for Interconnects with Large Number of Coupled Lines

SESSION 4

09:30 - 10:10

2.5D/3D Networks for High-Performance Applications

09:30

Andres Ayes, Eby G. Friedman

University of Rochester, USA

Power Integrity in 3-D Chiplet Systems with Intermediate Layers

09:50

Sriharini Krishnakumar, Inna Partin-Vaisband

University of Illinois Chicago, USA

Power-Integrity Modeling of VR Faults in High-Performance Applications

SPECIAL SESSION

10:40 - 12:00

History of SPI – 30th Anniversary

Speakers: **Flavio Canavero** (Politecnico di Torino, Italy); **Michel Nakhla** (Carleton University, Canada); **José Schutt-Ainé** (University of Illinois Urbana-Champaign, USA); **Madhavan Swaminathan** (Pennsylvania State University, USA); **Antonio Maffucci** (University of Cassino and Southern Lazio, Italy); **Mihai Telescu** (University of Brest, France); **Dries Vande Ginste** (Ghent University, Belgium)

Moderator: **Stefano Grivet-Talocia** (Politecnico di Torino, Italy)

## SESSION 5

13:30 - 15:10

## Crosstalk and EMC

13:30

Yutaka Uematsu (1), Kentaro Jumonji (2)*(1) Hitachi, Ltd., Japan; (2) Astemo, Ltd., Japan***A Shield-Assisted Dual-Side Common-Mode Choke Coils Architecture for Compact Automotive Ethernet ECUs**

13:50

Han-Ting Lin, Andreas Weisshaar*Oregon State University, USA***A Compact 8–18 GHz 150-ps True-Time-Delay Line in 0.18  $\mu\text{m}$  SiGe BiCMOS**

14:10

Min Kim, Shilong Zhang, Geuna Chang, Youngsoo Shin*Korea Advanced Institute of Science and Technology, South Korea***Signal-Integrity-Aware Routing and Shielding for UCIe-Compliant 2.5D ICs**

14:30

Jose Enrique Hernandez-Bonilla (1), Torben Wendt (1), Torsten Reuschel (2), Cheng Yang (3), Christian Schuster (3)*(1) Robert Bosch GmbH, Germany; (2) University of New Brunswick, Canada; (3) Hamburg University of Technology, Germany***Behavior of Crosstalk in Environmentally-Impacted Automotive PCB Interconnects and Effect on Signal Transmission**

14:50

Moritz Gappa (1), Burkhard Heinke (1), Cheng Yang (2), Christian Schuster (2)*(1) Airbus Operations GmbH, Germany; (2) Hamburg University of Technology, Germany***Systematic and Fast Crosstalk Modeling of 10Base-T1S Data Links in the Aircraft Cabin**

## SESSION 6

15:40 - 17:00

## High-speed Signal Integrity

15:40

Davit Kharshiladze (1), Hyunwook Park (1), Zhiping Yang (2), Chulsoon Hwang (1)*(1) Missouri University of Science and Technology, USA; (2) PCB Automation Inc., USA***Boosting High-speed Channel Transformer Performance with Gating Neural Network**

16:00

Mike Resso (1), Pratik Ghate (2), Tim Wang Lee (1), Rick Rabinovich (1)*(1) Keysight Technologies, USA; (2) FormFactor, Inc., USA***Signal Integrity Microprobing Strategies for Managing Channel Loss and Dense Packaging in AI Infrastructure Interconnects**

16:20

Andrew Josephson (1), Francesco de Paulis (2)*(1) Samtec, USA; (2) University of L'Aquila, Italy***Over-Moded Coaxial Test Cables for 425 Gbps PAM4 SerDes Validation Test Margin**

16:40

Si-Ping Gao (1,2), Jiahong Chen (1), Francesco de Paulis (3), En-Xiao Liu (4), Wenjian Yu (5)

(1) Nanjing University of Aeronautics and Astronautics, China; (2) Beijing National Research Center for Information Science and Technology, China; (3) University of L'Aquila, Italy; (4) A\*STAR IHPC, Singapore; (5) Tsinghua University, China

**Equivalent Circuit Modeling of Aperiodic On-Silicon PDNs for Fast What-If Analysis**

June 17, Wednesday

Energy Center

## SESSION 7

09:00 - 10:40

Advanced Design for Signal Integrity and Packaging

09:00

Gabriel Vaintrub (1), Grégory Houzet (1), Edouard Rochefeuille (1), David Auchere (2), Laurent Schwartz (2), Thierry Lacrevez (1)

(1) CROMA, CNRS, Univ. Savoie Mont-Blanc, France; (2) STMicroelectronics, France

**Development of a method for extracting the permittivity and permeability of molding compounds for IC packaging using a trident waveguide**

09:20

Shilong Zhang, Gyeongjin Kim, Youngsoo Shin

Korea Advanced Institute of Science and Technology, South Korea

**Fully Automated Thermal-Aware Trace Routing for Chip-on-Film Designs**

09:40

Taeho Park (1,2), SoYoung Kim (1)

(1) Sungkyunkwan University, South Korea; (2) Samsung Electronics Co., Ltd., South Korea

**A Methodology for Minimizing Driver Usage in High-Speed On-Chip Interconnects in Pre-Layout Phase**

10:00

Francesco Siconolfi (1), Daniele Pinchera (1), Luca Tari (1), Antonio Maffucci (1), Gabriele Cavaliere (2), Isaac Appiah Otoo (3), Maria Cojocari (3), Sarah Sibilgia (4), Francesco Cristiano (5), Gaspare Giovinco (1)

(1) University of Cassino and Southern Lazio, Italy; (2) University of Salerno, Italy; (3) University of Eastern Finland, Finland; (4) E-Lectra srl, Italy; (5) Nanesa srl, Italy

**A Multifunctional Graphene Coating for Advanced Electronic Packaging**

10:20

Antonio Maffucci (1,2), Ciro D'Elia (1,2), Alfredo Babusci (3), Andrea Gaetano Chiariello (4)

(1) University of Cassino and Southern Lazio, Italy; (2) EUT+ Institute of Nanomaterials and Nanotechnologies EUTINN, European Union; (3) Monozukuri spa, Italy; (4) University of Campania "L. Vanvitelli", Italy

**Signal Integrity Analysis of Integrated THz Graphene Antennas**

SESSION 8

11:10 - 12:30

Macromodeling and Model Order Reduction

11:10

Bijan Shahriari, Roni Khazaka

*McGill University, Canada*

**HIPPO-GRU Circuit Macro-Models based on Time- and Frequency-Domain Data**

11:30

Rayeed Rahman Ananda, Ramachandra Achar

*Carleton University, Canada*

**GPU-Accelerated Structure-Preserving Model Order Reduction of Large Multi-Port RLC Interconnects**

11:50

Owen Czuchra, Dries Peumans, John Lataire, Domenico Spina

*Vrije Universiteit Brussel, Belgium*

**Automatic Model-Based Characterization For Filter Design Verification**

12:10

Tommaso Bradde, Stefano Grivet-Talocia

*Politecnico di Torino, Italy*

**On Building  $\mathcal{D}$ -Stable Macromodels**

12:30 - 12:40

Closing Session

## European Hybrid IBIS Summit

14:00 - 18:00

28th IBIS Summit

*Program to be announced*