

INAUGURAL COURSE



GLOBAL SIGNAL INTEGRITY AND POWER INTEGRITY (SIPI) UNIVERSITY

Sunday, June 14, 2026 @ Castello del Valentino, Turin, Italy



JUNE 14-17
TURIN, ITALY

30th IEEE WORKSHOP
ON SIGNAL AND
POWER INTEGRITY



The **Global Signal Integrity and Power Integrity (SIPI) University** was successfully introduced by the **IEEE EMC Society** at the [EMC+SIPI 2024](#) in Phoenix, AZ, USA, and, following high demand, held for a second time at the [EMC+SIPI 2025](#) in Raleigh, NC, USA. Continuing its tradition of excellence, the program will once again offer its comprehensive two-day curriculum at the [2026 IEEE International Symposium on EMC+SIPI](#) in Dallas, TX, USA.

In a spirit of close collaboration and advancing technology worldwide, the **IEEE EMC Society**, in partnership with the **IEEE EPS** and the **SPI 2026 Organization**, will inaugurate the **Global SIPI University** at the **2026 IEEE Workshop on Signal and Power Integrity (SPI)**, to be held in Turin, Italy, bringing this premier educational experience to a wider international audience and ensuring another year of intensive, top-quality learning across both continents.

COURSE OVERVIEW

Modern high-speed digital systems are rapidly increasing in complexity as data rates climb and power distribution demands intensify. These unprecedented challenges require dedicated expertise in Signal Integrity (SI) and Power Integrity (PI), skills that are critically sought after by industry but are often scarce in traditional academic programs.

The **Global SIPI University @ SPI 2026** will be a focused, one-day intensive course, outlined to equip students, technicians, and engineers with further tools to bridge this crucial skills gap. Attendees will dive deep into SI & PI core concepts, learning directly from experienced and renowned instructors drawn from both industry and academia. The carefully curated curriculum aims to balance fundamental theory with direct practical application, covering analytical methods, simulation tools, and measurement techniques for solution validation.

FURTHER INFORMATION

Global SIPI University @ SPI 2026



G-SIPI-U @ SPI 2026

spi-workshop.org/global-sipi-university

SPI 2026 Website



IEEE SPI Workshop

spi-workshop.org

Email & Social Media



spi2026@polito.it



[linkedin/ieee-spi-workshop](https://www.linkedin.com/company/ieee-spi-workshop)



[instagram/ieee_spi_workshop](https://www.instagram.com/ieee_spi_workshop)



Christian Schuster

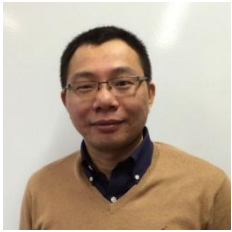
Hamburg University of Technology, Germany



Francesco de Paulis

University of L'Aquila, Italy

INSTRUCTORS & PROGRAM



Xiaomin Duan

IBM Research and
Development GmbH,
Ehningen, Germany

Keynote

SI and PI challenges for enterprise server design

In recent years, enterprise server deployment growth is exponential, fueled by AI acceleration, cloud-native computing, and heterogeneous workloads. These systems now demand extreme bandwidth densities and power delivery capabilities, often exceeding multi-terabit signaling and multi-kilowatt power envelopes. Such requirements place profound challenges in signal integrity (SI) and power integrity (PI) design. This keynote will examine the SI and PI challenges inherent to modern server design, with emphasis on high-speed interconnects, advanced packaging technologies, and power delivery networks. In particular, this talk will show how physical constraints such as board real estate, mechanical limits, and cost-performance trade-offs influence design decisions. It will include practical cases, highlighting co-design strategies, modeling techniques, and system-level optimization approaches. The goal is to foster a deeper understanding of how SI/PI methodologies evolve to meet the demands of next-generation computing infrastructure.



Francesco de Paulis

University of L'Aquila,
L'Aquila, Italy

Introduction to SI & PI

Evolution from the basics to the current technology

This presentation will introduce the concepts of signal and power integrity, and the evolution, in the past two decades, of the challenges associated with the modeling, analysis, and design of high speed interconnects and high-current PDNs. An overview of the current trends based on the state of the art of the technology discussed in the following sessions will be given.



Andreas Hardock

Nexperia Germany GmbH,
Hamburg, Germany

Signal Integrity I

Lumped vs. distributed discontinuities, transmission line effects, crosstalk & losses

As data rates and edge speeds in modern electronic systems continue to rise, the distinction between lumped and distributed discontinuities becomes critical for accurate signal-integrity and electromagnetic-compatibility design. This presentation gives an overview of how geometric and material transitions within interconnects behave either as localized impedance discontinuities or as electrically long structures exhibiting full transmission-line effects. Key mechanisms — including reflections, standing waves, and frequency-dependent propagation — are discussed to illustrate when traditional lumped-element approximations break down. The study further examines how distributed coupling paths give rise to near-end and far-end crosstalk, emphasizing the impact of trace geometry, dielectric properties, and return-path configuration. Additionally, conductor and dielectric losses are discussed in the context of attenuation, phase distortion, and their influence on high-speed waveform integrity. By integrating these phenomena into a unified perspective, the presentation highlights practical design considerations for minimizing signal degradation and ensuring robust performance across high-frequency interconnects.

Signal Integrity II

3D modeling and simulation, circuit modeling and simulation, equalization



Wendem Beyene

Meta Platforms,
Sunnyvale CA, USA

3D electromagnetic modeling and simulation, circuit-level modeling and simulation, and equalization are foundational to modern electronic system design, particularly for high-speed and high-frequency applications. When applied in an integrated manner, these techniques enable accurate performance prediction, early identification of signal- and power-integrity challenges, and systematic design optimization prior to physical prototyping—significantly reducing development time, cost, and overall technical risk. This presentation will highlight the successful design of modern SoCs and ASICs for wearable devices and infrastructure systems supporting AI workloads. As these designs incorporate both in-package and external memories with high-speed I/O interfaces and therefore require comprehensive electromagnetic analysis and circuit-level simulation. The discussion will include detailed system-level modeling and analysis methodologies used to optimize end-to-end performance across the complete signal and power delivery paths.

Signal Integrity III

VNA Measurements in Signal Integrity



Giordano Mariani

Rohde & Schwarz,
Milan, Italy

Signal integrity has become a critical aspect of modern high-speed digital design, today more than ever as data rates continue to rise and reliable transmission become essential. In this seminar, we will understand how VNAs are used to identify potential signal integrity issues and address them using tools and applications integrated in the network analyzer. First, we will cover the basics of VNA parameters and time domain analysis, which is necessary to gain the correct insights about my DUT. Then we will discuss the topic of de-embedding and see how it can help the designer make the correct choices when developing his PCB. We will end this presentation with a live demo of our VNA in action, including real measurements of transmission lines.

Power Integrity

SoC On-Die Power Integrity Basics



Gianni Signorini

Apple, Munich,
Germany

Modern System-on-Chip (SoC) designs are highly optimised to accommodate an increasing number of transistors and components within the smallest possible feature size. To ensure robustness and reliability, these advanced implementations require precise pre-silicon analysis methodologies. Power Integrity is the discipline that studies the quality of Power Delivery Networks (PDNs), ensuring that Power/Ground connections for each transistor of an SoC meet specific design targets that guarantee functionality. This presentation will provide an overview of the concepts and general principles of SoC On-Die Power Integrity simulations for a generic digital SoC. The talk will also provide insights on SoC Physical Design, Power Grid implementation, SoC Power calculation and its optimization.

Application Perspective

SI and PI aware design of automotive interconnects



Peter Hank

NXP Semiconductors GmbH, Hamburg, Germany



Aman Gupta

The necessity of further improved EMC/ESD/SIPI behavior and optimized PCB design is obvious, because high-complexity products with enhanced safety/security requirements need to be managed. Advanced PCB's with BGA-IC packages, high-speed clock lines with rich spectral-content, high-frequency signals with sharp rise-times and high slew-rates, often require an increased number of stacked PCB layers. To benefit from leading-edge technology processes and functions, many IC's require several voltage-rails and an optimized PDN, allowing reliable Inter-Chip connections along with proper communication between Electrical Control Units. This presentation provides an overview of most current challenges and gives an outlook how the complexity and the challenges can be managed, while meeting cost and time to market constraints under the harsh conditions of automotive applications.

SCHEDULE

TIME	TOPIC	INSTRUCTOR(S)
09:00 – 09:30	<i>On-site Registration</i>	
09:30 – 09:45	Opening	Francesco de Paulis & Christian Schuster
09:45 – 10:30	Keynote SI and PI challenges for enterprise server design	Xiaomin Duan
10:30 – 11:00	<i>Coffee Break / Networking</i>	
11:00 – 11:45	Introduction to SI & PI Evolution from the basics to the current technology	Francesco de Paulis
11:45 – 12:30	Signal Integrity I Lumped vs. distributed discontinuities, transmission line effects, crosstalk & losses	Andreas Hardock
12:30 – 14:00	<i>Lunch Break / Networking</i>	
14:00 – 14:45	Signal Integrity II: 3D modeling and simulation, circuit modeling and simulation, equalization	Wendem Beyene
14:45 – 15:30	Signal Integrity III VNA measurements in Signal Integrity	Giordano Mariani
15:30 – 16:00	<i>Coffee Break / Networking</i>	
16:00 – 16:45	Power Integrity SoC On-Die Power Integrity Basics	Gianni Signorini
16:45 – 17:30	Application Perspective SI and PI aware design of automotive interconnects	Peter Hank & Aman Gupta

REGISTRATION

Capacity is strictly limited to 100 attendees. Early registration is recommended to secure a place.

Global SIPI University Registration Fees		EARLY BIRD until March 27, 2026	STANDARD March 28, 2026, onwards *
Attendees registered also for SPI	Regular	€ 100	€ 150
	Student	€ 50	€ 75
Attendees registered only for G-SIPI-U	Regular	€ 200	€ 250
	Student	€ 100	€ 125

* Due to capacity limits, the Registration process may close at any time after this date. On-site registration may not be available.

ALL FEES INCLUDE

Full access to the course program • Lunch and coffee-breaks (Sunday)
Instructors presentation slides (PDF format) • Certificate of attendance (PDF format)